Time-to-Digital Converter
SC-TDC-1000 S Series
(Release 012, 013, 022 & 042)

Manual

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User Manual for the
SC-TDC-1000 S Series
Releases: 012, 013, 022 & 042
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1 Table of Contents


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2 General Information

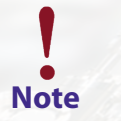
2.1 General Information

This manual is intended to assist users in the operation of the Releases 012, 013, 022, 023 and 042 in sub-releases 10, 85 and E8 of the SC-TDC-1000 S series. It is divided into 6 chapters. The chapter "General Information" contains a brief overview of the devices as well as the safety instructions. The chapter "Installation" refers to installation and cabling. The other chapters contain amongst others technical details and the description of the device layout.

2.2 Safety Instructions

Please read this manual carefully before performing any electrical or electronic operations and strictly follow the safety rules given within this manual. Surface Concept declines all responsibility for damages or injuries caused by an improper use of the module due to negligence on behalf of the User.

The following symbols may appear throughout the manual:



The "note symbol" marks text passages, which contain important information/hints about the operation of the detector. Follow these information to ensure a proper functioning of the detector.

The "caution symbol" marks warnings, which are given to prevent an accidental damaging of the detector or the readout system. Do NOT ignore these warnings and follow them strictly. Otherwise no guarantee is given for arose damages.

The "high voltage symbol" marks warnings, given in conjunction with the description of the operation/use of high voltage supplies and/or high voltage conducting parts. Hazardous voltages are present, which can cause serious or fatal injuries. Therefore only persons with the appropriate training are allowed to carry out the installation, adjustment and repair work.

Please also respect the Surface Concept Device Safety Instructions Manual in addition and all given safety rules within it.

2.3 General Overview of the System

The Surface Concept SC-TDC-1000 S device in Release 012 is a 8 stop input channel (08S) and in Release 022 a 16 stop input channel (16S) Time-to-Digital Converter with an integrated FPGA board and a USB3.0 interface in a stand alone table top housing. The SC-TDC-1000 S device in Release 013 is comparable to the R012 but comes in a 19“ rack mount housing.
The devices in sub-releases 10 and 85 come with basic functionalities, while the devices in sub-release E8 come with additional inputs (like TAG IN, ADC IN) for an extended measurement functionality.
The SC-TDC-1000 S Series is laid out for low voltage (LV)TTL signals on BNC connectors for all inputs and outputs. All LVTTL signal inputs are TTL tolerant.

The SC-TDC-1000 S device in Release 042 is a special version of the Release 022 with modified start and stop input channels. It is laid out for NIM signal levels on LEMO 00 type connectors for all stop and the start inputs. All additional input signals are still laid out for LVTTL signal levels on BNC connectors. The SC-TDC-1000 S device in Release 042 is only available in sub-release 10 (see **Chapter 4.2**).

Do not open the device, while it is in operation. Hazardous voltages are present. In case that the device must be opened, turn off the device first AND pull out the power plug.

3 Installation

3.1 Initial Inspection

Visual inspection of the system is required to ensure that no damage has occurred during shipping. Should there be any signs of damage, please contact our provider immediately. Please check the delivery according to the packing list (see **Table 1**) for completeness.

- SC–TDC-1000 S (R012, R013, R022, R042)
- 1x USB cable
- 1x power cable

Table 1: Packing list for the SC-TDC-1000 S (R012, R013, R022, R042)

3.2 Cabling

The general connection scheme of the SC-TDC-1000 S devices is given in **Figure 1**.

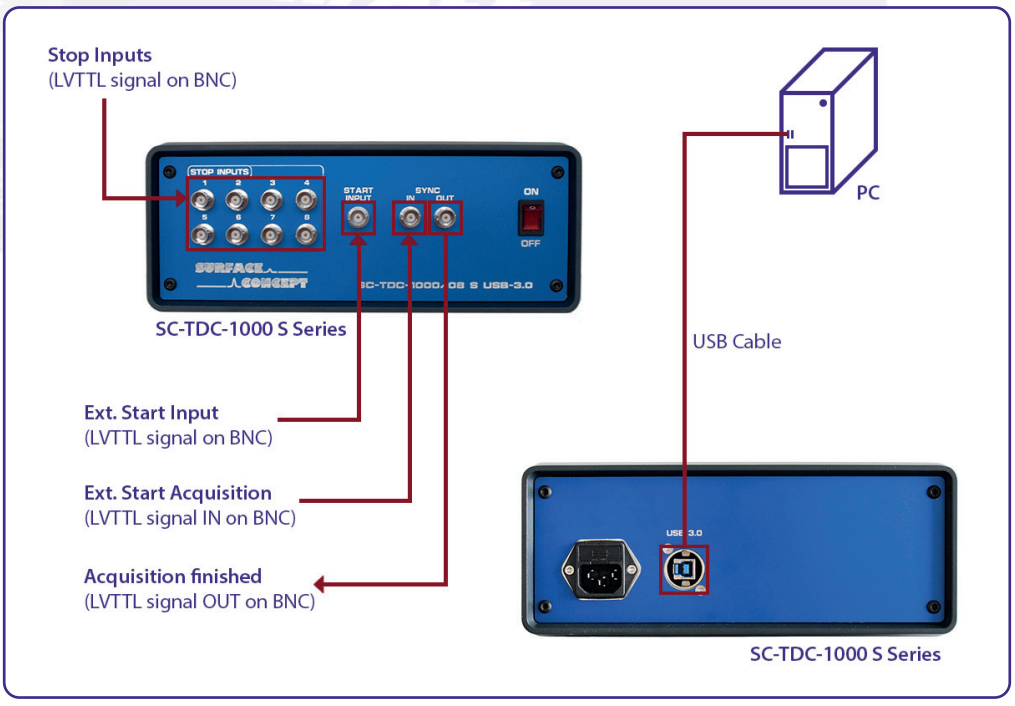


Figure 1: General connection scheme of the SC-TDC-1000 S devices.

For release versions 012, 013 & 022

- Use the BNC sockets named "Stop" to apply 1 - 8 (R012, R013) and 1 - 16 (R022) LVTTL signals to the TDC stop input channels.
- To perform time measurements with respect to an external clock, provide start pulses to the start input of the TDC. Use the BNC socket named "Start" to apply LVTTL signals (see **Chapter 4.2.2** for detailed information).
- Use the USB cable to connect the TDC to the PC. Do not use PC front panel USB connectors; they are often restricted in performance (see **Chapter 3.3** for further details).
- Connect the power cable to the main connector.
- Install the TDC device driver or software package prior to switching on the TDC.

For release version 042

- Use the LEMO 00 sockets named "Stop" to apply 1 - 16 NIM signals to the TDC stop input channels.
- To perform time measurements with respect to an external clock, provide start pulses to the start input of the TDC. Use the LEMO 00 socket named "Start" to apply NIM signals (see **Chapter 4.2.2** for detailed information).
- Use the USB cable to connect the TDC to the PC. Do not use PC front panel USB connectors; they are often restricted in performance (see **Chapter 3.3** for further details).
- Connect the power cable to the main connector.
- Install the TDC device driver or software package prior to switching on the TDC.

For sub-release versions 10, 85 & E8

- Use BNC cables to connect your additional signals to the additional inputs of the TDC (e.g. SYNC IN or TAG IN).
- Please note that all additional inputs are internally 50Ohm terminated and are laid out for 50Ohm terminated LVTTL (low voltage TTL) signal levels.

Finish the complete cabling before the TDC is turned on and the GUI software is started. Also, close the software and turn off the TDC before performing any changes to the cabling.
This applies especially to the connection and disconnection of the start input of the TDC. The start input of the TDC cannot handle pulses which are arriving in a time interval of smaller than 120ns, as they are produced by e.g. connecting to and disconnecting from the start input respectively.
If two subsequent pulses are applied to the start input of the TDC, the device will still deliver results, but these results will contain wrong timing information.

3.3 Software Installation, Requirements and Interface

All operation functions of the SC-TDC-1000 S devices are encapsulated in a dynamic linked library (scTDC1.dll). Data processing and presentation on the PC is realized by an end-user demo software. See the corresponding software manual for detailed information on the software package and the DLL interface.

The delivery package of the SC-TDC-1000 S devices includes a storage medium with hardware drivers and a TDC Demo software. Connect the storage medium to your PC and install the software package as described in the Software Installation Manual.

Read-out of the TDC is done with a standard PC via USB3.0. For the PC the following minimum system requirements are highly recommended:

- Processor: Quad Core
- RAM: 4GB
- Windows 7 or higher
- USB (no front panel connector)

Note

Depending on the specific PC system used for the TDC readout (mainly depending on the specific USB3.0 chip used on the PC motherboard), the use of USB3.0 can lead to instabilities in the data communication. For those cases we then recommend the use of USB2.0. The use of USB2.0 is always possible, but there might be limitations in the maximum count rates for certain detector types and/or detector operation modes.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4 TDC Layout

4.1 Schematic Description of the SC-TDC-1000 S Devices

The design of the SC-TDC-1000 S series combines the excellent performance of the GPX TDC chip with a high speed USB interface.

A field programmable gate array (FPGA) enables comfortable setups and a variable data stream handling from the TDC via USB.
The main delayline detector readout functionality is permanently programmed. A complex FIFO design makes data losses almost impossible. The user DLL controls the data handling and streaming for the user.

The following brief description of the internal structure of the measurement unit is only informative:

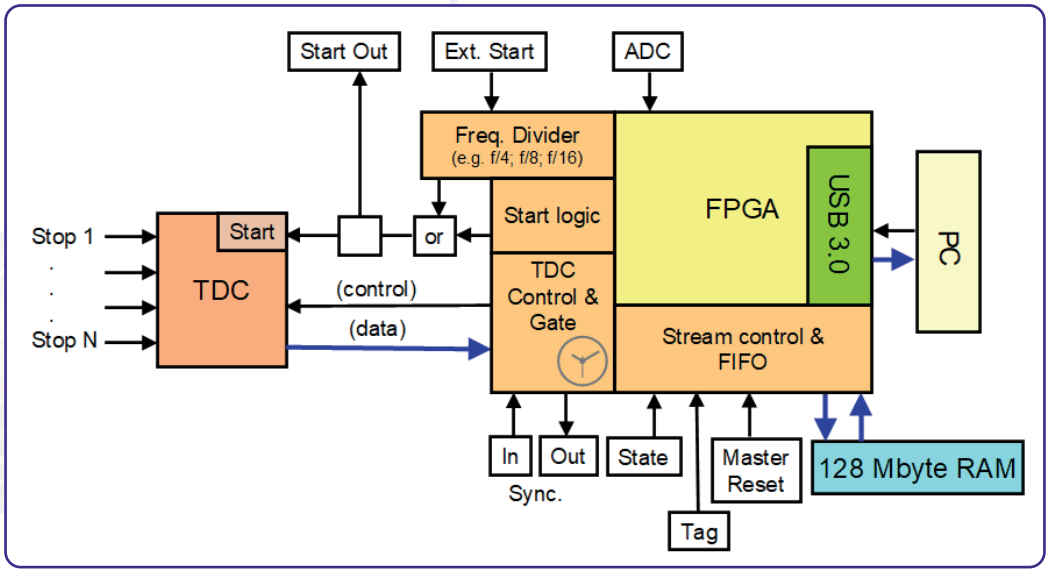

Figure 2: Schematic sketch of TDC functioning.

Arrival times of pulses at the stop inputs are measured by the TDC with respect to either an internal reference start signal, provided by the FPGA, or an external start signal. An internal electronics provide the TDC start signal to an additional BNC socket for further extended measurement use. The measurement dwell times for data from the TDC are settled within the FPGA by a quartz stabilized time gate in an interval from 1ms to 1193h.
The synchronization pulse for the external acquisition start (SYNC IN) is transferred directly into the FPGA that controls the acquisition process. The FPGA also sends out a synchronization pulse for marking the end of an acquisition (via the SYNC OUT).

Additional inputs (e.g. TAG or ADC) are available (sub-R E8) to feed in additional signals directly into the TDC data stream for extended measurement functionality.

The TDC data streaming can be performed with a specific pre-conditioning of the DLD data, which includes channel pairing, pair result arithmetic and many more. Communication to and from the PC is achieved via a USB interface. Data streaming via the USB interface is provided without losses using a large memory buffer within the device.

4.2 Layout of the SC-TDC-1000 S Series

Figure 3: Layout of the SC-TDC-1000/08S R012-10

1. BNC Sockets for Stop Inputs (R012, 013 & 022), LEMO Sockets for Stop Inputs (R042)
2. BNC Socket for Start Input (R012, 013 & 022), LEMO Socket for Start Input (R042)
3. BNC Sockets for Device Synchronization Signal IN and OUT
4. Power switch to turn the TDC ON/OFF. Lighted, when set to ON
5. Power Socket
6. USB Connection Socket

4.2.1 TDC Stop Inputs

The SC-TDC-1000 S devices come with 8 (R012, R013) or 16 (R022, R042) stop input channels. All stop signals must be applied as LVTTL (minimum amplitude of at least +2.1V on 50Ohms) signals to the "STOP INPUTS" (BNC socket). There is an exception for the R042, where all stop signals must be applied as NIM signals to the "STOP INPUTS" (LEMO 00 socket).

4.2.2 TDC Start Input

An external start signal must be provided to the TDC for real time resolved measurements. The external start signal must be applied as a LVTTL (minimum amplitude of at least +2.1V on 50Ohms) signal to the "START INPUT" (BNC socket) for R012, R013 and R022 and as NIM signal to the "Start Input" (LEMO 00 socket) for R042. In addition the software must be set to accept external start signals, by changing the corresponding entry in the tdc_gpx3.ini file.

The corresponding entry in the tdc_gpx3.ini file is:

Ext_Gpx_Start = X

X is either NO or YES. **The default setting is YES**.
"Ext_Gpx_Start" = YES must be set for the TDC to accept the external start signal.
In addition the following entries in the tdc_gpx3.ini must be set as follows:

StartCounter = YES
StartPeriod = 0x800000

Measurements are performed in respect to an internal start signal of the TDC when "Ext_Gpx_Start" = NO. This internal start signal has no time correlation to any external clock and therefore also not to the incoming stops. Any external start signal must be disconnected from the start input of the TDC, when working with the internal start signal.
The rise time of the start signal is of great importance, the faster the rise time, the better the time resolution. The maximum frequency of the start pulse must not exceed 7MHz.

Do not forget to save the ini file after any changes you make and restart the software. For further information check the software manual.

Note

Take care that measurements are performed either with the internal start signal (Ext_Gpx_Start = NO) and no signal applied to the Start Input or with an external start signal (Ext_Gpx_Start = YES) applied to the Start Input. In all other cases the TDC is not working correctly.

The start input of the TDC cannot handle pulses which are arriving in a time interval of smaller than 120ns (e.g. as produced by connecting/disconnecting the start signal during TDC operation). If two such subsequent pulses are applied to the start input of the TDC, the device will still deliver results, but these results might contain wrong timing information.

The TDC does also not work with start signals of frequencies larger than 7MHz. For this reason, the TDCs are equipped with an internal frequency divider. Larger start pulse frequencies must be divided down by an appropriate dividing factor (e.g. dividing factor of 16 for 80MHz start pulse frequency). For start frequencies smaller then 100kHz the user must make sure that all stop signals are provided within a time window of 10.7µs after each start. Otherwise the TDC will deliver wrong time results, which are not easy to be identified as such.
For applications with time distances larger 10.7µs use the start counter or the extended measurement range (see Chapter 4.2.6).

Note

The temporal resolution is mainly influenced by the quality of the start signal because the TDC measures the time of a rising or a falling edge using a constant voltage threshold. Lower precision than expected may be observed for slow rise or fall times of the signals or in case of any ripple/jitter on the switching edge of the signals. In particular, the time resolution may distinctively depend on any voltage variation of the ground level of the measured start signal.
Therefore, if the signals are varying in amplitude, one needs to process them by external electronics components (e.g. constant fraction discriminators, CFDs).

4.2.3 TDC Start Output (sub-R 85 and E8 only)

The TDC holds an internal electronics, which provide the TDC start signal for further extended measurement use. The "START OUT" (BNC socket) provides either the external start if applied or the internal start, generated by the FPGA.

4.2.4 Device Synchronization Signal IN/OUT

The data acquisition can be synchronized to an external signal for various measurement application linked to external devices. This device synchronization signal has to be applied as LVTTL signal to the "SYNC IN" (BNC socket) of the TDC. This functionality is switched on/off within the tdc_gpx3.ini file.

The corresponding entry in the tdc_gpx3.ini file is:

Ext_trigger = X

X is either NO or YES. **The default setting is NO**.
The TDC ignores any external synchronization signals if "Ext_trigger" = NO. In case that "Ext_trigger" = YES and the "SYNC IN" signal is not provided, the device will not come to operation at all.

The TDC provides always a LVTTL signal on the "SYNC OUT" (BNC socket) after the end of each acquisition, independent on the setting of "Ext_trigger".

Note

Do not forget to save the ini file after any changes you make and restart the software. For further information check the software manual.

4.2.5 Start Frequency Divider (sub-R 85 and E8 only)

The maximum start frequency for the SC-TDC-1000 S devices is restricted to 7MHz. To cope with larger start frequencies the SC-TDC-1000 S devices are equipped with an internal start frequency divider for external start frequencies of up to 150MHz (this mode only works when using the external start input). Herewith the frequency divider can operate with different dividing factors, which can be set within the software, to always guarantee a start frequency of below 7MHz.
The frequency divider is switched on/off within the tdc_gpx3.ini file, in which also the dividing factors are set.
The corresponding entry in the tdc_gpx3.ini file is:

Start_Divider = X

X is an integer value and must be one of the following values: 0, 2, 4, 8, 16 or 32. The value 1 is not allowed.
The default setting is 0
X = 0 switches off the start divider and leads to normal operation without dividing the start frequency.

The time histogram will appear X times in series, when using a dividing factor of X. This is due to the fact that only each 1st start pulse out of a sequence of X start pulses will be accepted as start signal, while all stop signals are detected. This leads to the multiple time histograms that appear sequentially in time. The multiple histograms can be resorted to one single time histogram by a MODULO-operation during data analysis.

4.2.6 Extended Measurement Range (sub-R 85 and E8 only)

The measurement range in the normal start-stop operation mode is 10.7µs. The SC-TDC-1000 S devices can be equipped with an extended measurement range functionality, to cope with larger measurement ranges .The reference measurement is switched on/off within the tdc_gpx3.ini file.

The corresponding entry in the tdc_gpx3.ini file is:

ReferenceMeasurement = X

X is either NO or YES. **The default setting is NO**.
X = NO switches the reference measurement off.

The extension of the measurement range is working in such a way, that start signals are internally counted up to extend the global time axis. For this the TDC is operating with its internal start signal, while the external start signal is given to one of the stop signals in addition to the regular stop signals. Time results are then provided as reference results of the external start and the stop signals on basis of the internal extended time axis.
Therefore one of the stop inputs of the TDC must be used to apply the external start signal, which reduces the number of available stop inputs by one.
Additional changes in the tdc_gpx3.ini file must be made for the extended measurement range to function.

The corresponding entries in the tdc_gpx3.ini file to be made are:

Ext_Gpx_Start = NO
StartCounter = NO
StartPeriod = 0

It must also be defined in the tdc_gpx3.ini file which of the stop input channels provide the reference signal for calculating the times of the other stop signals. The need of defining the reference channel also allows to define different reference channels for the different stop channels.

The corresponding entry in the tdc_gpx3.ini file is:

ReferenceChannelX = Y

X corresponds to the specific number of the stop channel. **Y** defines the specific stop channel which is used for stop channel X as reference channel. The channel numbering starts with 0. Single channels can also be switched off in case that signals on that channel should not be measured itself, but only be used as reference channel. In this case X can be set to -1.
The reading of this entry is: "the reference of channel X is channel Y".

Example 1

ReferenceChannel0 = -1
ReferenceChannel1 = 0
ReferenceChannel2 = 0
…..
ReferenceChannel# = 0

represents the maximum available channel number.
With this definition all applied stop signals are measured in reference to the signal applied to channel 1 (0 in the software channel counting), while the signals of channel 1 themselves are not measured.

Example 2

ReferenceChannel0 = -1
ReferenceChannel1 = 0
ReferenceChannel2 = 2
ReferenceChannel3 = 2

With this definition the stop signal on channel 2 is measured in reference to the signal applied to channel 1 while the stop signal on channel 4 is measures in reference to the signal applied to channel 3. Also the signals of channel 1 themselves are not measured, but the signals of channel 3 are measured in reference to themselves. With such definition the results from channel 3 provide the time between two subsequent signals on channel 3 (in case that this signal is a periodic signal, the time result represents exactly that period).

It can happen that the use of more than one stop channel can lead to a wrong sorting of events within the data stream in respect to their time while using the extended measurement range functionality. This behaviour can be corrected by a sorting algorithm that resorts neighbouring signals within a certain "depth". This depth can be adjusted in the tdc_gpx3.ini file.

The corresponding entry in the tdc_gpx3.ini file is:

ChronoDepth = X

X is an integer value and must be set between 0 and 8.
The default setting is 0
X = 0 switches off the sorting algorithm.
The sorting algorithm works better at higher selected values, but higher values significantly increase the load on the PC CPU.

4.2.7 Tag Signal Input (sub-R E8 only)

The tag input is an additional counter input for signal counting. The counter number is included into the general data stream of the TDC. The tag signal has to be applied as a LVTTL (low voltage TTL) signal on 50Ohms to the "TAG IN" (BNC socket) of the TDC.
In addition changes in the tdc_gpx3.ini file must be made for the tag signal to be registered by the TDC.

The corresponding entry in the tdc_gpx3.ini file is:

TimeTag = X

X is an integer value and must be one of the following values: 0, 1, 2, 3, 4, 5 or 6.
The default setting is 0.
Each value represents a certain functionality, which is described below:

TimeTag = 0 ;tag counting is switched off and any signal to the "TAG IN" is ignored, nBytes can be set to 4 or 8 (see below for further details on nBytes). Also any state input, master reset input or ADC input signals are ignored.

TimeTag = 1 ;the tag is counting the internal 80MHz clock signal of the FPGA and is therefore functioning as a timer. Any signal to the "TAG IN" is ignored. This mode is not working in combination with the state input.

TimeTag = 2 ;the tag is counting the external LVTTL signal applied to the "TAG IN". The counter is reset with the start of a new measurement. This mode is not working in combination with the state input.

TimeTag = 3 ;tag counting is switched off and any signal to the "TAG IN" is ignored. This value must be set for using the ADC functionality in combination with the state input and the master reset input.

TimeTag = 4 ;corresponds to the setting of TimeTag = 3.

TimeTag = 5 ;must be set for using the tag as timer (similar to TimeTag = 1) but in combination with the state input. A pulse on "Tag In" resets the timer to 0.

TimeTag = 6 ;must be set for using the tag as counter (similar to TimeTag = 2) but in combination with the state input.

The number of bits which are available for each detector event (x, y, t) is defined by an additional parameter called "nBytes" in the tdc_gpx3.ini file.

The corresponding entry in the tdc_gpx3.ini file is:

nBytes = X

X is an integer value of either 4 or 8. **The default setting is 8**.

Different settings of "nByte" parameter in combination with different settings of the "TimeTag" parameter results in a further differentiation of the TimeTag functionality as described below:

"nBytes" = 4 ;each detector event x, y, t has a length of 32bit. The sub-definition for the different coordinates x, y and t is defined by the "DataFormat" (e.g. "DataFormat" = 2 ;x = 11bit, y = 11bit, t = 10bit, see the software manual for further details).

"nBytes" = 8
"TimeTag" = 0 ;each detector event x, y, t has a length of 64bit. The sub-definition for the different coordinates x, y and t is defined by the "DataFormat" (e.g. "DataFormat" = 2 ;x = 11bit, y = 11bit, t = 42bit, see the software manual for further details).

"nBytes" = 8
"TimeTag" > 0 ;each detector event x, y, t has a length of 64bit. The first 32bit are used for the tag counter. The second 32bit are sub-definition for the different coordinates x, y and t is defined by the "DataFormat".
In case that "TimeTag" > 0, "nBytes" is set to 8 automatically within the software and any ini file settings are ignored.

4.2.8 Master Reset Input (sub-R E8 only)

The master reset input is treated as an additional sign signal within the TDC and is counted up in a software counter within the dll.
In addition the master reset input is connected to the reset pin of the TDC chip. Each time a signal is applied to the master reset input the corresponding software counter is counting up and the input and output FIFOs of the TDC chip are cleared (all old TDC data are erased).
A LVTTL (low voltage TTL) signal on 50Ohms has to be applied to the "MASTER RESET IN" (BNC socket) of the TDC.

4.2.9 State Signal Input (sub-R E8 only)

The state signal has to be applied as a LVTTL (low voltage TTL) signal on 50Ohms to the "STATE IN" (BNC socket) of the TDC.
In addition, the value of the variable named "TimeTag" in the tdc_gpx3.ini file (depending on the software version which is used) must be adapted for the state/sign signal to be registered by the TDC.
The state or sign signal input assumes values 0 or 1, depending on the given electronic level of the LVTTL signal (low or high).
For the state/sign input to be functioning the following variables in the tdc_gpx3.ini must be used:

TimeTag = 3 ;must be set for using the state/sign input in combination with the ADC functionality and the master reset input. The tag counting is switched off and any signal to the "TAG IN" is ignored.

TimeTag = 4 ;corresponds to the setting of TimeTag = 3

TimeTag = 5 ;must be set for using the state/sign input. Hereby the state/sign input functions in combination with the tag signal functioning as a timer, counting the internal 80MHz clock signal of the FPGA. A signal on "TAG IN" resets the timer to 0.

TimeTag = 6 ;must be set for using the state/sign input. Hereby the state/sign input functions in combination with the tag signal functioning as a counter, counting the external LVTTL signal applied to the "TAG IN".

4.2.10 ADC Input (sub-R E8 only)

The SC-TDC-1000 S devices with sub-release E8 come with an integrated 14bit Analog-to-Digital converter with a differential signal input ("ADC IN +" and "ADC IN -") which is laid out for analog voltages between +10V and -10V.
To work with the ADC the value of the variable named "TimeTag" in the tdc_gpx3.ini file must be adapted in the following way:

TimeTag = 3 ;must be set for using the ADC functionality. This will work also in combination with the state/sign input and the master reset input. The tag counting is switched off and any signal to the "TAG IN" is ignored.

TimeTag = 4 ;corresponds to the setting of TimeTag = 3

In case that no differential analogue signal would be available, one can also use a single non-differential signal. In this case one has to use the positive input ("ADC IN +") of the ADC, while terminating the negative input ("ADC IN -") to ground. Please be aware that this way of operating is working, but it is more prone to noise.

5 Technical Data

SC-TDC-1000/08S - Release 012-10 & 013-10

- 2HE table top housing with 254mm x 272mm x 106mm (w/d/h) (R012)
- 19" 3HE Rack Mount Housing (R013)
- Number of Stop Inputs: 8
- Number of Start Inputs: 1 (common start input usable as reset of the internal clock resolution adjust mode: quartz-accurate, adjustable resolution, insensitive to temperature variations, adjustable via software (no calibration necessary)
- Digital time bin resolution per channel: 82.3ps
- 5.5ns pulse-pair resolution on one channel and 0ns between two channels
- Trigger to rising edge
- Start retrigger frequency (max.): 7MHz
- Measurement range: 0ns – 10.7µs in start-stop operation
  (measurement range of 10.7µs corresponds to a start frequency of 93.5kHz)
- Dynamic range: 2E19
- All channels provide precisely an equal resolution
- 32-fold multi-hit capability per channel
- 40MHz internal device measurement rate
- Stop Signal Input: Low voltage TTL on 50Ohm BNC socket
- External Start Signal Input: Low voltage TTL on 50Ohm BNC socket
- Device Synchronization Signal Input: Low voltage TTL on 50Ohm BNC socket
- Device Synchronization Signal Output: Low voltage TTL on 50Ohm BNC socket
- USB Interface for Data Transfer

SC-TDC-1000/08S - Release 012-85 & 013-85

- 2HE table top housing with 254mm x 272mm x 106mm (w/d/h) (R012)
- 19" 3HE Rack Mount Housing (R013)
- Number of Stop Inputs: 8
- Number of Start Inputs: 1 (common start input usable as reset of the internal clock resolution adjust mode: quartz-accurate, adjustable resolution, insensitive to temperature variations, adjustable via software (no calibration necessary)
- Digital time bin resolution per channel: 82.3ps
- 5.5ns pulse-pair resolution on one channel and 0ns between two channels

- Trigger to rising edge
- Start retrigger frequency (max.): 7MHz
- Measurement range: 0ns – 10.7µs in start-stop operation
  (measurement range of 10.7µs corresponds to a start frequency of 93.5kHz)
- Extended measurement range of up to 82.3ps x 64bit (>17000d) in reference mode
- Internal start frequency divider (2-, 4-, 8-, 16- and 32-fold divider)
- Dynamic range: 2E19
- All channels provide precisely an equal resolution
- 32-fold multi-hit capability per channel
- 40MHz internal device measurement rate
- Stop Signal Input: Low voltage TTL on 50Ohm BNC socket
- External Start Signal Input: Low voltage TTL on 50Ohm BNC socket
- External Start Signal Output: Low voltage TTL on 50Ohm BNC socket
- Device Synchronization Signal Input: Low voltage TTL on 50Ohm BNC socket
- Device Synchronization Signal Output: Low voltage TTL on 50Ohm BNC socket
- USB Interface for Data Transfer

SC-TDC-1000/08S - Release 012-E8 & 013-E8

- 2HE table top housing with 254mm x 272mm x 106mm (w/d/h) (R012)
- 19" 3HE Rack Mount Housing (R013)
- Number of Stop Inputs: 8
- Number of Start Inputs: 1 (common start input usable as reset of the internal clock resolution adjust mode: quartz-accurate, adjustable resolution, insensitive to temperature variations, adjustable via software (no calibration necessary)
- Digital time bin resolution per channel: 82.3ps
- 5.5ns pulse-pair resolution on one channel and 0ns between two channels
- Trigger to rising edge
- Start retrigger frequency (max.): 7MHz
- Measurement range: 0ns – 10.7µs in start-stop operation
  (measurement range of 10.7µs corresponds to a start frequency of 93.5kHz)
- Extended measurement range of up to 82.3ps x 64bit (>17000d) in reference mode
- Internal start frequency divider (2-, 4-, 8-, 16- and 32-fold divider)
- Dynamic range: 2E19
- All channels provide precisely an equal resolution
- 32-fold multi-hit capability per channel
- 40MHz internal device measurement rate
- Stop Signal Input: Low voltage TTL on 50Ohm BNC socket
- External Start Signal Input: Low voltage TTL on 50Ohm BNC socket

- Device Synchronization Signal Input: Low voltage TTL on 50Ohm BNC socket
- Device Synchronization Signal Output: Low voltage TTL on 50Ohm BNC socket
- Tag, State/Sign and Master Reset Input: Low voltage TTL on 50Ohm BNC socket
- ADC Input: 14bit ADC with differential analogue signal input (+/-10V) on BNC sockets
- USB Interface for Data Transfer

SC-TDC-1000/16S - Release 022-10

- 2HE table top housing with 254mm x 272mm x 106mm (w/d/h)
- Number of Stop Inputs: 16
- Number of Start Inputs: 1 (common start input usable as reset of the internal clock resolution adjust mode: quartz-accurate, adjustable resolution, insensitive to temperature variations, adjustable via software (no calibration necessary)
- Digital time bin resolution per channel: 82.3ps
- 5.5ns pulse-pair resolution on one channel and 0ns between two channels
- Trigger to rising edge
- Start retrigger frequency (max.): 7MHz
- Measurement range: 0ns – 10.7µs in start-stop operation
  (measurement range of 10.7µs corresponds to a start frequency of 93.5kHz)
- Dynamic range: 2E19
- All channels provide precisely an equal resolution
- 32-fold multi-hit capability per channel
- 80MHz internal device measurement rate
- Stop Signal Input: Low voltage TTL on 50Ohm BNC socket
- External Start Signal Input: Low voltage TTL on 50Ohm BNC socket
- Device Synchronization Signal Input: Low voltage TTL on 50Ohm BNC socket
- Device Synchronization Signal Output: Low voltage TTL on 50Ohm BNC socket
- USB Interface for Data Transfer

SC-TDC-1000/16S - Release 022-85

- 2HE table top housing with 254mm x 272mm x 106mm (w/d/h)
- Number of Stop Inputs: 16
- Number of Start Inputs: 1 (common start input usable as reset of the internal clock resolution adjust mode: quartz-accurate, adjustable resolution, insensitive to temperature variations, adjustable via software (no calibration necessary)
- Digital time bin resolution per channel: 82.3ps
- 5.5ns pulse-pair resolution on one channel and 0ns between two channels
- Trigger to rising edge

- Start retrigger frequency (max.): 7MHz
- Measurement range: 0ns – 10.7µs in start-stop operation
  (measurement range of 10.7µs corresponds to a start frequency of 93.5kHz)
- Extended measurement range of up to 82.3ps x 64bit (>17000d) in reference mode
- Internal start frequency divider (2-, 4-, 8-, 16- and 32-fold divider)
- Dynamic range: 2E19
- All channels provide precisely an equal resolution
- 32-fold multi-hit capability per channel
- 80MHz internal device measurement rate
- Stop Signal Input: Low voltage TTL on 50Ohm BNC socket
- External Start Signal Input: Low voltage TTL on 50Ohm BNC socket
- External Start Signal Output: Low voltage TTL on 50Ohm BNC socket
- Device Synchronization Signal Input: Low voltage TTL on 50Ohm BNC socket
- Device Synchronization Signal Output: Low voltage TTL on 50Ohm BNC socket
- USB Interface for Data Transfer

SC-TDC-1000/16S - Release 022-E8

- 2HE table top housing with 254mm x 272mm x 106mm (w/d/h)
- Number of Stop Inputs: 16
- Number of Start Inputs: 1 (common start input usable as reset of the internal clock resolution adjust mode: quartz-accurate, adjustable resolution, insensitive to temperature variations, adjustable via software (no calibration necessary)
- Digital time bin resolution per channel: 82.3ps
- 5.5ns pulse-pair resolution on one channel and 0ns between two channels
- Trigger to rising edge
- Start retrigger frequency (max.): 7MHz
- Measurement range: 0ns – 10.7µs in start-stop operation
  (measurement range of 10.7µs corresponds to a start frequency of 93.5kHz)
- Extended measurement range of up to 82.3ps x 64bit (>17000d) in reference mode
- Internal start frequency divider (2-, 4-, 8-, 16- and 32-fold divider)
- Dynamic range: 2E19
- All channels provide precisely an equal resolution
- 32-fold multi-hit capability per channel
- 80MHz internal device measurement rate
- Stop Signal Input: Low voltage TTL on 50Ohm BNC socket
- External Start Signal Input: Low voltage TTL on 50Ohm BNC socket
- External Start Signal Output: Low voltage TTL on 50Ohm BNC socket
- Device Synchronization Signal Input: Low voltage TTL on 50Ohm BNC socket

- Device Synchronization Signal Output: Low voltage TTL on 50Ohm BNC socket
- Tag, State/Sign and Master Reset Input: Low voltage TTL on 50Ohm BNC socket
- ADC Input: 14bit ADC with differential analogue signal input (+/-10V) on BNC sockets
- USB Interface for Data Transfer

SC-TDC-1000/16S - Release 042-10

- 2HE table top housing with 254mm x 272mm x 106mm (w/d/h)
- Number of Stop Inputs: 16
- Number of Start Inputs: 1 (common start input usable as reset of the internal clock resolution adjust mode: quartz-accurate, adjustable resolution, insensitive to temperature variations, adjustable via software (no calibration necessary)
- Digital time bin resolution per channel: 82.3ps
- 5.5ns pulse-pair resolution on one channel and 0ns between two channels
- Trigger to rising edge
- Start retrigger frequency (max.): 7MHz
- Measurement range: 0ns – 10.7µs in start-stop operation
  (measurement range of 10.7µs corresponds to a start frequency of 93.5kHz)
- Dynamic range: 2E19
- All channels provide precisely an equal resolution
- 32-fold multi-hit capability per channel
- 80MHz internal device measurement rate
- Stop Signal Input: NIM on 50Ohm LEMO 00 socket
- External Start Signal Input: NIM on 50Ohm LEMO 00 socket
- Device Synchronization Signal Input: Low voltage TTL on 50Ohm BNC socket
- USB Interface for Data Transfer

Line Input

Electrical Input (LINE)	85 V – 260 V, 50/60 Hz
Power	65 Watt (max.)
Fuse	1x T 1.6 A


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6 List of Figure

EC Declaration of Conformity

Manufacturer

Surface Concept GmbH
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CE

Product SC-TDC-1000 Series

The above named products comply with the following European directive:

89/336/EEC	Electromagnetic Compability Directive, amended by 91/263/ EEC and 92/31/ EEC and 93/68/EEC
73/23/EEC	Low Voltage Equipment Directive, amended by 93/68/EEC

The compliance of the above named product to which this declaration relates is in conformity with the following standards or other normative documents where relevant:

EN 61000-6-2:2005+AC:2005	Electromagnetic compatibility (EMC): Generic standards - Immunity for industrial environments
EN 61000-6-4:2007+A1:2011	Electromagnetic compatibility (EMC): Generic standards - Emission standard for industrial environments
EN 61010-1: 2010	Safety Requirements for Electrical Equipment for Measurement, Control and Laboratory Use

For and on behalf of **Surface Concept GmbH**

Mainz,……01.04.2013……. (Date)

Legal Signature…… (Dr. Andreas Oelsner)

This declaration does not represent a commitment to features or capabilities of the instrument. The safety notes and regulations given in the product related documentation must be observed at all times.